REMARKS

Claims 1 - 39 are pending in this broadening reissue application. The Applicant has amended claims 18, 23, 35, and 36.

The Applicant has added no new matter to the reissue application.

In light of the foregoing, claims 1 – 17, 19 – 22, 24 – 34, and 37 - 39 as previously pending, and claims 18, 23, and 35 – 36 as amended are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 16th day of November, 2001.

Respectfully submitted,

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MARKED UP VERSION OF AMENDED SPECIFICATION AND CLAIMS

Abstract:

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the synchronous integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch [(flip-flop)] flip-flop element of the integrated circuit device is loaded with data and is allowed to conduct: a slave latch [(flip-flop)] flip-flop element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct.

Paragraphs beginning at Column 1, line 6 and ending at Column 2, line 6:

The subject matter of the present application is related to [copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993] U.S. Pat. No. 5,577,051, titled "Improved Static Memory Long Write Test", [attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993] U.S. Pat. No. 5,835,427, titled "Stress Test Mode", [attorney docket no. 93-C-56] all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following [pending U.S. patent applications] U.S. patents by David Charles McClure entitled:

"Architecture Redundancy", [Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136)] U.S. Pat. No. 5,612,918, and

"[()]Redundancy Control", [Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143), which were both filed on Dec. 29, 1995] U.S. Pat. No. 5,790,462, which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are [arguable] arguably related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709 [Attorney's Docket No. 95-C-137)],

Ser. No. 09/457,558 which is a continuation of Ser. No. 08/587,709,

Ser. No. 09/454,800 which is a divisional of Ser. No. 08/587,709,

"Pipelined Chip Enable Control Circuitry and Methodology", [Ser. No. 08/588,730_(Docket No. 95-C-138)] U.S. Pat. No. 5,701,275,

U.S. Pat. No. 5,798,980 which is a divisional of U.S. Pat. No. 5,701,275,

"Output Driver Circuitry Having a Single Slew Rate Resistor", [Ser. No. 08/588,988 (Docket No. 95-C-139)] U.S. Pat. No. 5,801,563,

"Synchronized Stress Test Control", [Ser. No. 08/589,015 (Docket No. 95-C-142)] U.S. Pat. No. 5,712,584,

"Write Pass Through Circuit", [Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144)] U.S. Pat. No. 5,657,292,

"Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", [Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145)] U.S. Pat. No. 5,845,059,

"Synchronous Output Circuit", [Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146)] U.S. Pat. No. 5,619,456,

"Write Driver Having a Test Function", [Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147)] U.S. Pat. No. 5,745,432,

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 [(Attorney's Docket No. 95-C-148)] (since abandoned),

U.S. Pat. No. 5,808,960 which is a continuation of Ser. No. 08/589,139,

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 [(Attorney's Docket No. 95-C-149)] (since abandoned),

U.S. Pat. No. 5,825,691 which is a continuation of Ser. No. 08/588,737,

"Clocked Sense Amplifier with Wordline Tracking", [Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150)] U.S. Pat. No. 5,802,004,

U.S. Pat. No. 5,828,622 which is a divisional of U.S. Pat. No. 5,802,004,

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 [(Attorney's Docket No. 95-C-151)] (since abandoned),

U.S. Pat. No. 5,848,018 which is a continuation of Ser. No. 08/589,140,

"Device and Method for Isolating Bit Lines from a Data Line", [Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154)] U.S. Pat. No. 5,691,950,

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", [Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156)] U.S. Pat. No. 5,864,696,

U.S. Pat. No. 6,006,339 which is a divisional of U.S. Pat. No. 5,864,696,

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", [Ser. No. 08/589,024,] U.S. Pat. No. 5,619,466 [(Attorney's Docket No. 95-C-168],

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 [(Attorney's Docket No. 169] (since abandoned),

U.S. Pat. No. 5,896,336 which is a continuation of Ser. No. 08/587,708,

U.S. Pat. No. 5,883,838 which is a divisional of Ser. No. 08/587,708,

and the following [pending U.S. patent applications] U.S. patents by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 [(Attorney's Docket No. 95-C-141)] (since abandoned),

U.S. Pat. No. 5,805,523 which is a continuation of Ser. No. 08/589,023,

"Switching Master/Slave Circuit", [Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03) U.S. Pat. No. 5,783,958,

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.

Paragraph at Column 2, line 63:

Therefore, according to the present invention, the entire data path of the synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch [(flip-flop)] flip-flop element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch [(flip-flop)] flip-flop element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct.

Paragraph at Column 3, line 45:

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the

integrated circuit device in th t st mode, a clock signal (either an external clock signal of an associated internal clock signal) is internally clocked. As the clock signal go s to a low logic state upon power-up of the device, a master latch [(flip-flop)] flip-flop element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch [(flip-flop)] flip-flop element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct. Using the present invention, both the master and slave latch elements are sequentially loaded with the correct data state [and then allowed to sequentially conduct].

Paragraph at Column 4, line 35:

Control bar derivative signal [14] 23 from Node 4 and Control derivative signal [18] 27 from Node 3 control TTL cell 22 shown in FIG. 1a. TTL cell 22 contains the following elements: p-channel MOS transistors 50, 52 and 58 and N-channel MOS transistors 54, 56 and 60. The gates of transistors 50 and 60 are supplied with Control bar signal [14] 23. The gates of transistors 52 and 54 are supplied with Clock signal 12, and the gates of transistors 56 and 58 are supplied with the Control signal [18] 27. A first source/drain of transistor 50 and a first source/drain of transistor 58 are connected to power supply voltage Vcc as shown. A second source/drain of transistor 50 is connected to a first source/drain of transistor 52. A second source/drain of transistor 52 is connected to a first source/drain of transistor 54, a first source/drain of transistor 60 and a second source/drain of transistor 58 to form output signal [23] 21 on Node 5. A second source/drain of transistor 54 is connected to a first source/drain of transistor 56. A second source/drain of transistor 56 is connected to a second source/drain of transistor 60 and power supply voltage Vss.

Paragraphs beginning at Column 4, line 66 and ending at Column 6, line 2:

Referring once more to FIG. 1a, during power-up in a periphery stress test mode, Control' bar derivative signal 23 (shown at Node [3] 4 of FIG. 1) and Control' derivative signal 27 (shown at Node [4] 3 of FIG. 1) are both a low logic state and signal 21 at Node 5 is forced to a high logic state. This gives the appearance that Clock input signal 12 was a low logic state. Convers ly, when the Power-On-Reset signal 16 goes to a

low logic state, and when Control' bar derivative signal 23 and Control' derivative signal 27 [go to] remain at high logic states, signal 21 is forced to a low logic state which gives the appearance that Clock signal 12 was a high logic state. Thus, a high logic state on controls signals Control' bar derivative signal 23 and Control' derivative signal 27 during a periphery stress test mode forces the equivalent of a high going clock input. During a memory cell stress test mode, the equivalent of a low going clock input is forced. Upon power-up of the device, Power-On-Reset signal 16 goes high and Clock derivative signal [12] 38 is forced to a low logic state during which the master latch of the device is loaded with data and allowed to conduct. Following completion of the power-on reset cycle, Power-On-Reset signal 16 does low and data is latched into the master latch; also data is loaded into the slave latch [which is allowed to device conduct]. Using the circuitry of FIG. 1a, the state of Clock derivative signal [12] 38 is forced to the desired logic state during a test mode, either a periphery stress test mode or a memory cell stress test mode.

The operation of FIG. 1a to force the condition of the Clock derivative signal [12] 38 as desired may be further illustrated with reference to a second input buffer circuit. Referring to FIG. 2, a schematic diagram of an address input buffer 70, according to the preferred embodiment of the present invention, is shown. Input buffer 70 includes the following elements: TTL (transistor transistor logic) cell 22, inverters 74, 88, 92 and 94, and passgates 90 and 96. The details of TTL cell 22 are similar to those shown in FIG. 1a. Input buffer 70 contains a master latch 95 comprised of elements inverter 92, inverter 94 and [passgate] passgates 90 and 96. Input buffer 70 is supplied with the following input derivative signals: Clock signal 38, Control bar signal 14, IN data signal 15, Control signal 18 and Clock bar signal [13] 21 and generates output signal 98.

When Control bar signal 14 and Control signal 18 are both a high logic state, signal 72 at Node 1 is a low logic state. Because of the way the TTL cell of FIG. 1a forces Clock derivative signal 38 to the desired logic state. Clock derivative signal 38 is initially a low logic state but will ultimately go to a high logic state so that the master latch 95 initially conducts, thereby forcing signal 98 to a [high] low logic state. Clock signal [12] 38 will then go to a high logic state, [turning off] thus latching master latch 95.

Signal 98 propagates to Row Address Driver circuitry 100 of FIG. 3, according to th preferred embodiment of the invention. Row address driver circuitry 100 is composed of inverters 110, 112, 114, 124 and 126, p-channel MOS transistor 118, n-

channel MOS transistor 122, and passgate 120. Signal 98 from FIG. 1 is provided to a series of inverters 110, 112 and 114 which delay and [inverter] invert signal 98 to produce Row Address signal 116. Signal 98 is also presented to passgate 120 which is controlled by Address Override-P signal 104 and Address Override-N signal 106. The output signal of passgate 120 is pulled up towards Vcc by p-channel transistor 118 whose gate is controlled by Rows On bar signal 102 and is pulled down towards Vss by n-channel transistor 122 whose gate is controlled by Rows Off signal 108. The output signal of passgate 120 passes through two inverters 124 and 126 to become Row Address bar signal 128. Row Address bar signal 128 is the inverse of Row Address signal 116. Rows On bar signal 102 forces Row Address bar signal [116] 128 on (in an asserting condition) when it is a low logic state in the test mode and Rows Off signal 108 forces Row Address bar signal [116] 128 off (not in an asserting condition) when it is a high logic state in the test mode. P-channel MOS transistor 118 and n-channel MOS transistor 122 act as row address override devices in the test mode.

Paragraphs beginning at Column 6, line 17 and ending at Column 6, line 44:

The Row Address signal 116 generated by FIG. 3 feeds the Word Line and Block Select Latch circuitry 130 shown in FIG. 4, according to the preferred embodiment of the invention. In addition to Row Address signal 116, circuitry 130 is supplied with Smart Clock signal 132, Smart Block Select signal 134, Block Address0 signal 136, Block Address1 signal 138 and Block Address2 signal 140, and Reset signal 192. Circuitry 130 generates Row signal 190 and Block Select bar signal 194. Smart Clock signal 132 is a high-going narrow pulse generated from the rising edge of Clock derivative signal [12] 38 and Smart Block Select signal 134 is a derivative signal of Smart Clock signal 132. The elements of circuitry 130 include: inverters 142, 146, 148, 150, 154, 164, 166 and 186; passgates 144, 152 and 162; NAND logic gate 160; p-channel MOS transistors 156, 168, 170, 172; and n-channel MOS transistors 158, 174, 176, 178, 180, 182 and 184.

Row Address signal 116 is supplied by FIG. 3 to the input terminal of inverter 142. Smart Clock signal 132 is provided to a control terminal of both passgates 144 and [152] 162 as shown and accordingly controls passgates 144 and [152] 162; it additionally is provided to the input terminal of inverter 150. Smart Block Select signal 134 is an input signal to passgate 152 which is indirectly controlled by Block Address

signals 136, 138 and 140. Block Address0 signal 136 is provided to the gates of transistors 168, 174 and 184. Block Address1 signal 138 is provided to the gates of transistors 178, 170 and 180. Block Address2 signal 140 is provided to the gates of transistors 182, 172 and 176.

Paragraphs beginning at Column 6, line 52 and ending at Column 7, line 7:

Following the powering-up of the integrated circuit device which is controlled by Power-On-Reset signal 16, Power-On-Reset signal 16 goes low and Clock derivative signal [12] 38 goes from a low logic state to a high logic state. This also causes Smart Clock signal 132 to go to the high logic state since Smart Clock signal 132 is a derivative signal of Clock derivative signal [12] 38, as previously discussed. A high logic state of Smart Clock signal 132 causes slave latch member 144 to load in data supplied by Row Address signal 116 and to conduct. Thus, the conduction of slave latch 144 follows the conduction of the master latch of FIGS. 1 and 1a.

The Row signal 190 and Block Select bar signal 194 generated by circuitry 130 are supplied to Word Line Select circuitry 200 of FIG. 5, according to the preferred embodiment of the present invention. In addition to signals 190 and 194 circuitry 200 is provided with Row bar signal 202, which is the inverse of Row signal 190. The elements of circuitry 200 include NOR logic gates 204 and 208; and inverters 206, 210 and 212. Circuitry 200 produces signal Row Driver Line even bar signal 218, Row Driver Line odd bar signal 216 and Block Select signal [216] 214 (the inverse signal of Block Select bar signal 194).

Claims 18, 23, 35, and 36:

18. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

generating a second data bit from the first data bit;

latching the first data bit in the master latch [after powering up the integrated circuit]; and

loading the second data bit into a slave latch [after powering up the integrated circuit].

23. Th method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state [stage].

35. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

latching the first data bit in the master latch [after powering up the integrated circuit]; and

loading the first data bit into a slave latch [after powering up the integrated circuit].

36. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state [stage].

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